AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A jitter reducing apparatus, comprising:

an elastic store that stores data received from a synchronous digital hierarchy (SDH) network;

a pattern generator that controls a data read speed so the elastic store maintains a constant amount of stored data;

a modulation sequencer that ~~generates~~ outputs signals representative of a digital signal wave having a constant period and amplitude, wherein the output signals include a signal indicative of an amplitude of the digital signal wave and a signal indicative of a direction of the digital signal wave; and

a phase level detector that controls the pattern generator ~~using the digital signal wave~~ based on the signals output from the modulation sequencer.

2. (Currently Amended) The apparatus of claim 1, wherein the phase level detector further controls the pattern generator using a difference value between the amount of stored

data in the elastic store and an amount of data outputted from the elastic store~~, less a value of the digital signal wave~~.

3. (Currently Amended) The apparatus of claim 1, wherein the phase level detector is operated at time intervals upon receipt of the ~~digital signal wave~~ signals from the modulation sequencer.

4. (Original) The apparatus of claim 1, wherein the pattern generator performs a controlling operation of a pattern generation speed at regular time intervals.

5. (Original) The apparatus of claim 1, wherein the modulation sequencer is operated upon receipt of an 8KHz frame pulse and a 6.48MHz clock frequency.

6. (Original) The apparatus of claim 5, wherein the modulation sequencer generates the digital signal wave of which one period is 16 sections of the frame pulse and has a 500 Hz bandwidth.

7. (Original) The apparatus of claim 1, wherein the modulation sequencer outputs a mode-value signal indicative of an amplitude level of the digital signal wave and a mode-slope signal indicative of a positive and a negative direction of the digital signal wave.

8. (Original) The apparatus of claim 7, wherein the mode-slope signal controls a positive section or a negative section of the digital signal wave.

9. (Currently Amended) The apparatus of claim 7, wherein the mode-value signal ~~repeats~~ comprises one of four signal values of 00, 01, 10, and 11.

10. (Original) The apparatus of claim 7, wherein the mode-value signal and the mode-slope signal implement a binary code signal with a high voltage level and a low voltage level.

11. (New) An apparatus comprising:

an elastic store device to store data;

a pattern generator to control a data read speed from the elastic store device so as to maintain an approximately constant amount of stored data;

a phase level device to control the pattern generator; and

a modulation sequencer to output signals representative of a digital signal wave to the phase level device, the output signals including at least an amplitude signal and a slope signal.

12. (New) The apparatus of claim 11, wherein the phase level device controls the pattern generator based on the signals output from the modulation sequencer and a difference between the amount of stored data in the elastic store and an amount of data outputted from the elastic store device.

13. (New) The apparatus of claim 11, wherein the elastic store device stores data received from a synchronous digital hierarchy network.

14. (New) The apparatus of claim 11, wherein the modulation sequencer outputs a mode-value signal indicative of an amplitude level of the digital signal wave and a mode-slope signal indicative of a positive direction or a negative direction of the digital signal wave.

15. (New) The apparatus of claim 14, wherein the mode-slope signal controls a positive section or a negative section of the digital signal wave.

16. (New) The apparatus of claim 14, wherein the mode-value signal comprises one of four signal values of 00, 01, 10 and 11.

17. (New) The apparatus of claim 14, wherein the mode-value signal and the mode-slope signal implement a binary code signal with a high voltage level and a low voltage level.

18. (New) An apparatus comprising:

an elastic store device to store data;

a modulation sequencer device to output signals representative of a digital signal; and

a device to receive the signals output from the modulation sequencer device and to control a data read speed from the elastic store device, wherein the signals output from the modulation sequencer device include signals indicative of a slope of a digital signal or an amplitude of the digital signal.

19. (New) The apparatus of claim 18, wherein the modulation sequencer device outputs a mode-value signal indicative of an amplitude level of the digital signal and a mode-slope signal indicative of a positive direction or a negative direction of the digital signal.

20. (New) The apparatus of claim 19, wherein the mode-slope signal controls a positive section or a negative section of the digital signal.